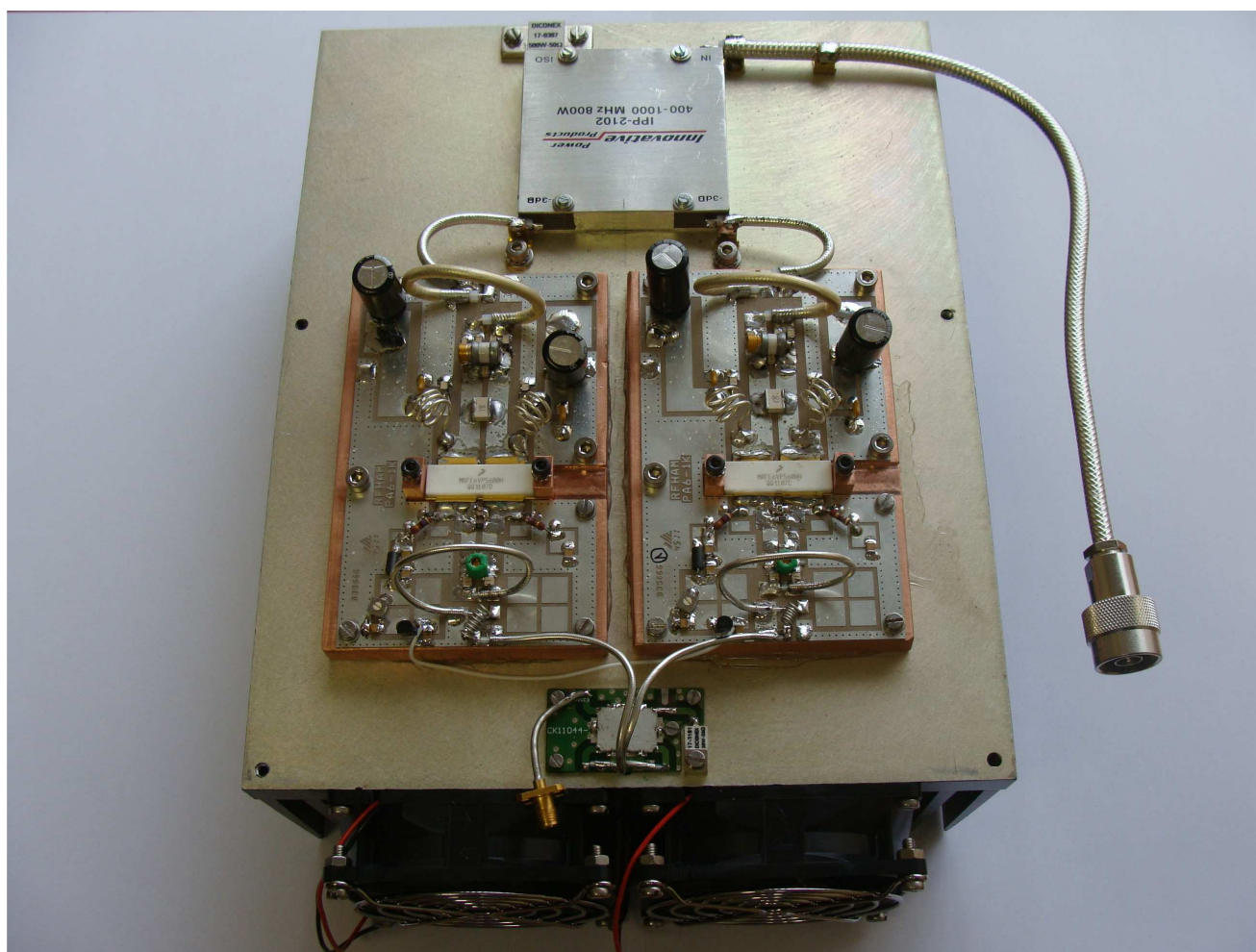


Compact 432 MHz 1 kW High Power Solid State Amplifier using 2 x MRF6VP5600H

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With the help of Remco den Besten PA3FYM

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This article describes an RF amplifier design using high power RF solid state devices. If you have no experience working with these high powers, please consult a qualified technician who has experience.

1. Introduction

Based on the article of Lionel F1JRD (AE7KX) and my article for 6 m, we were inspired to build a 70 cm 1kW SSPA module..

After some experiments with the MRFE6VP61K25H, I decided to make a pallet of ca. 600 W and combined two pallets in order to get 1 kW out.

Why ?

First of all, the output impedance of the 1K25 is very low (in the range of 1 Ω).

On 70 cm, for more than 600 W, components close to the first matching cells become very hot (due to the internal loss ESR) and the solder goes into “reflow”, and components will burn.

So, to have a good design to be reproduced, it is preferred to use 2 x MRFE6VP5600H.

The MRFE6VP5600H is a versatile device, well suited for a wide range of applications. It is capable of delivering 600 W under continuous wave conditions thanks to its high efficiency and low thermal resistance. The device handles high VSWR conditions.

This publication is focused on the 432 MHz radio amateur band for both analog and digital waveforms. (SSB or WSJT/FSK/CW)

Main characteristics of the amplifier :

Frequency band: 430 - 435 MHz

Output Power @ P3dB > 1000 W

Operating supply voltage: 50V

Gain typ > 20 dB

Eff typ > 60 %



MRFE6VP5600HR6

The MRFE6VP5600H is part of the Freescale 50 V product line, which is designed specifically for high voltage application for the RF Power market. It is fabricated using Freescale’s proprietary Very High Voltage 6th generation with enhanced ruggedness (VHV6E) platform. This technology is fully qualified and ships in large volumes.

2. Advantages of 50V Drain Voltage

Using a 50V device has great advantages compared to lower voltage devices because the output impedance of a 50V-device for the same output power is much larger, making the output matching circuitry easier and less lossy. Currents will also be lower compared to lower voltage devices.

50V LDMOS technology has better IMD performances compared to lower voltage devices , specially compared to 12V devices using bipolar technology.

These LDMOS devices can be fed using market standard drain 50 V-supplies (most are adjustable from ca. 43 to 54 V).

For other technical aspects, please refer to DUBUS issue 4 / 2010 vol 39 "Compact 144 MHz High Power Solid State Amplifier using MRFE6VP61K25H" from F1JRD/AE7KX

3. Amplifier design and performance

The goal of this module is to be able to get 1 kW solid state, with good efficiency, small size, and good VSWR-handling into operation.

The PCB for this pallet is the same as the 6 m pallet PA61K.
For thermal aspect is referred to (1).

The PCB is TC350 material, which has a very good RF and thermal performance.
The size of the amplifier is 120 x 72 mm.
The transistor has to dissipate more than 300 w in a small area, so a copper heat spreader is necessary to transfer the heat to the aluminum heat sink.

Two techniques can be used to put the PCB on the copper heat spreader:
With screws like in the picture, or with solder.
This last technique needs some expertise and some solder paste (3).

Circuit description:

The input circuit is realized with 1:1 50Ω balun and a micro-strip matching lines towards the gates.

The input matching is tuned by L1, and C6.
The 500Ω trimmer can be removed if an external bias circuit is used.
1 K R2 and R4 are connected to ground to prevent a bias disconnection (if P1 is not in use)

The output circuit uses also micro-strip lines and a 50Ω balun, made of 50Ω .141 coaxial cable .
Particular attention has to be paid to soldering the capacitors C18,C9,C20,C21 (5.1 pF ATC 100 B or Temex CHB)
(see the picture).
One 18 pF high Q factor capacitor CLX series from TEMEX may replace the four 5.1 pF capacitors..

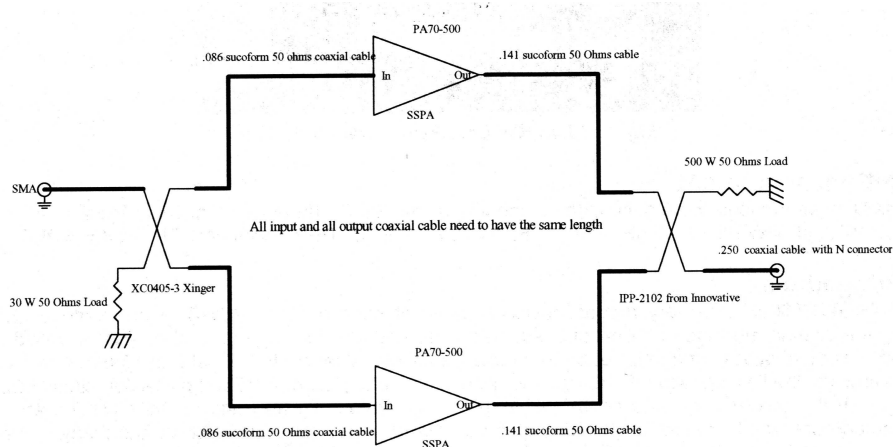
C23 is used to tune up for optimal efficiency.

In this amplifier I didn't use a balancing wire. This can be done, and it will improve 2 nd harmonic suppression.

In order to get a kW brick we need to combine two pallets.
Combining high powers is a precise issue and several techniques may be used.

I have chosen to use a -3 dB 90 ° hybrid coupler from Innovative using a IPP2102. This is an expensive part but very safe. This coupler is used to combine the two outputs of the two pallets.
At the input I used a -3 dB 90° hybrid coupler from Anaren XC0405-03.

Remco PA3FYM will describe in the next Dubus issue an alternative way to combine with a lower cost.



RF measurements were performed in CW

50 V Drain supply, 2 x 1000 mA Idq (For linear operation):
This test is done with the amplifier only (without filter)

Freq (MHz)	Pin (W)	Pout (W)	Gain (dB)	Drain Eff (%)	PAE(%) *	Vd (V)	Id1(A)	Id2(A)	P power supply (W)
432	1.5	200	21.2	28.8	28.6	47.7	7.2	7.4	694
432	2	300	21.8	35.8	35.6	47.6	8.7	8.9	838
432	2.7	400	21.7	41.1	40.8	47.5	10.1	10.4	974
432	3.5	500	21.5	45.8	45.5	47.3	11.4	11.7	1093
432	4.3	600	21.4	49.6	49.3	47.2	12.6	13	1209
432	5.4	700	21.1	53.2	52.8	47	13.8	14.2	1316
432	7	800	20.6	56.2	55.7	46.5	15.1	15.5	1423
432 1 dBc	8.8	900	20.1	58.9	58.3	46.3	16.3	16.7	1528
432	10.4	1000	19.8	60.8	60.1	46.1	17.6	18.1	1646
432	13.7	1100	19	62.7	62	45.9	18.8	19.4	1754

* PAE : Power Added Efficiency this value include the RF input power

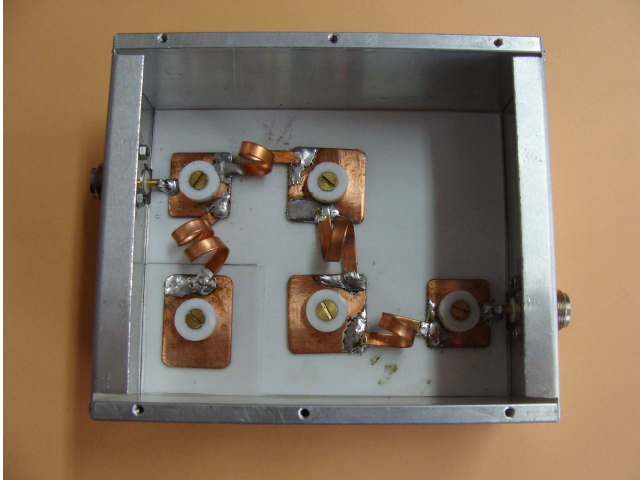
The harmonic test show H2 @ - 47 dBc and H3 @ - 83 dBc in 1296 MHz at 1 KW output power.

A filter is absolutely necessary to get the harmonics below 60 dBc.

Test with the filter

The harmonic test show H2 @ - 70 dBc and H3 @ - 86 dBc in 1296 MHz at 1 KW output power.

We have tested this amplifier with a filter, designed by F5CYS, based, on a F1TE design for 2 m (3), This filter has also a 2 m rejector to reduce the broadband noise in a multi VHF contest team.



F5CYS 70 cm kW power filter

5. IMD measurement

*The IMD measure was done in the same conditions as the 2 m amplifier (with 2 drivers)
Idq : 2 x 1A*

*Pout : 1200 W PEP
IMD3 : - 23 dBc / PEP*

*Pout : 800 W PEP
IMD3 : - 28 dBc / PEP*

*Pout : 400 W PEP
IMD3 : - 34 dBc / PEP*

7. Ruggedness

*MRFE6VP5600H is a very rugged device, capable of handling 65:1 VSWR in pulse mode.
It was designed for high mismatch applications, such as laser and plasma exciters, that exhibit repetitive high VSWR values at startup and then come back to a more friendly impedance.
In CW, at these VSWR levels and rated powers, the limiting factor is the maximum DC power dissipation.*

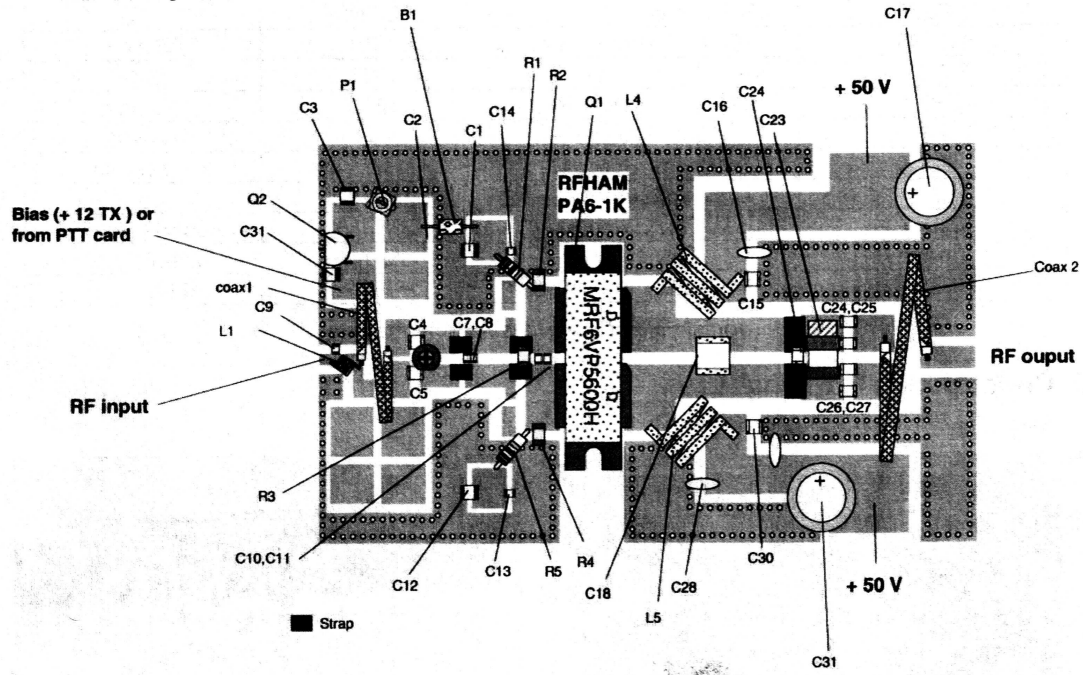
A VSWR protection circuit that will shutdown the gate voltage to 0 or -3V within 10mS on a single shot, will protect the transistor effectively.

The amplifier presented here was tested for all phase angles with 10mS pulses (5% duty cycle) without any failure or degradation in RF performance.

*In any case a protection circuit has to be used, like the ones described for the 6 m and 2 m amplifiers.
A circulator can be used also, but is expensive.*

Construction :

Layout and bill of material for one pallet.



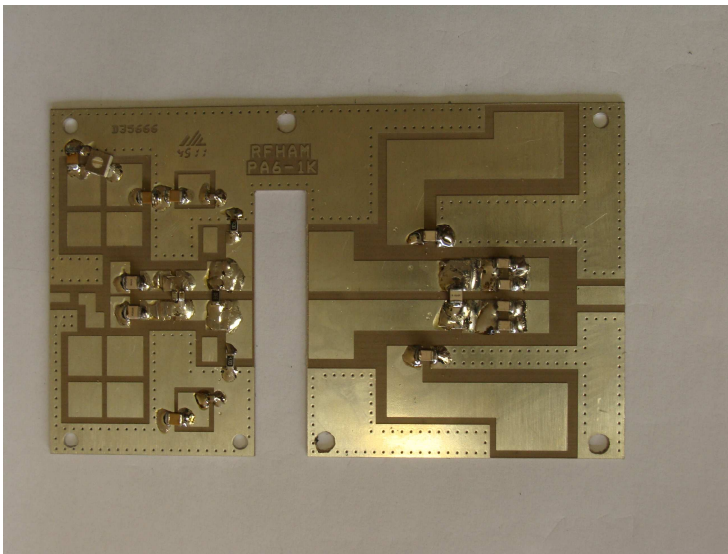
Fixture layout and placement

Tab1. Bill Of Materials

B1	Bead with wire Fair-Rite (95 ohm@100MHz)		
L1 (Air inductor)	6 Turn air inductor on 3 mm diameter,	Tinned copper wire of 0.6 mm diameter	
L4,L5 (Air inductor)	3 Turn air inductor on 7 mm diameter,	Silver plated copper wire of 12/10mm diameter	
C1,C2,C3,C12	100 nF Ceramic Capacitor 100 V	SMD	
C4,C5	39 pF Ceramic HQ Capacitor	100 B , CHB	ATC , TEMEX
C 6	Trimming capacitor 3 to 30 pF	Green	Murata(RF electronica CVC-30)
C7, C8	5.6 pF NPO or HQ	SMD	
C9	4.7 pF NPO or HQ	SMD	
C10,C11	33 pF Ceramic HQ Capacitor	100 A	ATC , TEMEX
C13,C14	1 nF NPO Ceramic Capacitor	SMD	
C15,C30	330 pF to 1 nF Ceramic HQ Capacitor	100 B , CHB	ATC , TEMEX
C16,C28	100 nF 100 V Ceramic Capacitor		LCC
C18	18 pF Ceramic HQ capacitor	CLX	TEMEX
	Or		
C18,C19,C20,C21	5.1 pF Ceramic HQ Capacitor	100 B , CHB	ATC , TEMEX
C23	Giga trimmer 1.3 to 16 pF	5476	Johanson (RF electronica CVG-N1)
C24	10 pF Ceramic HQ Capacitor	100 B , CHB	ATC , TEMEX
C24,C25,C26,C27	220 pF Ceramic HQ Capacitor	100 B , CHB	ATC , TEMEX
C17,C31	100 uF 160V		
C32	100 nF Ceramic Capacitor 100 V	SMD	
R1 ,R5	47 ohm 1 W Power Resistor	PR01	Vishay
R2 ,R4	470 ohm 1/4 W Power Resistor	1206	Vishay

R3	33 ohm 1/4 W Power Resistor	1206	Vishay
P1	500 Ohms SMD pot		Bourns
Q1	MRFE6VP5600H		Freescale
Q2	78L05	TO92	
Coax1	50 Ohm 11 cm	SM.086	Huber & Suhner
Coax2	50 Ohm 11 cm	SM.141	Huber & Suhner
PCB	Arlon TC350, 2 OZ 30 mils	PA6-1K	RFham.com

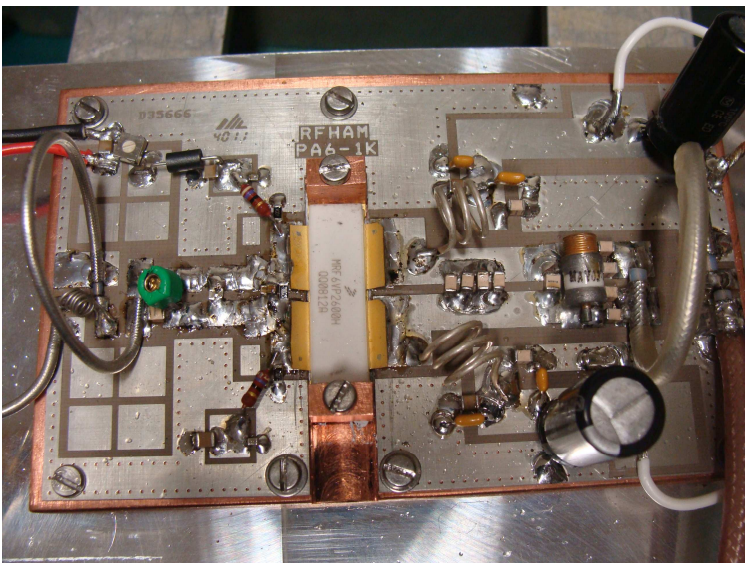
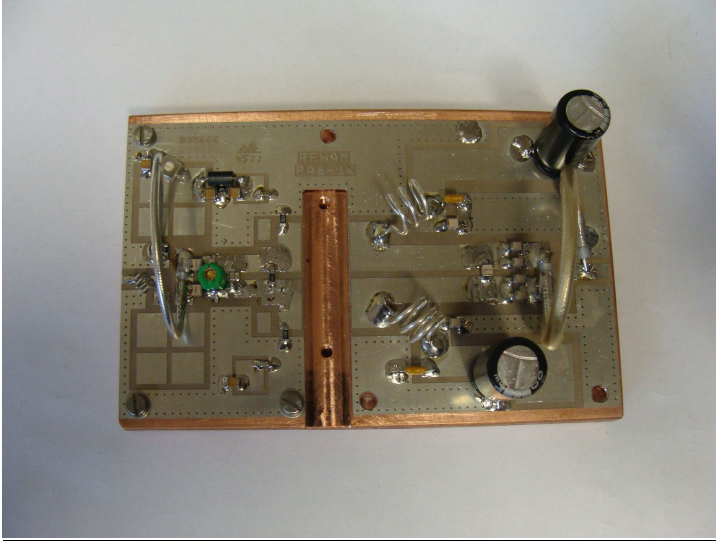
1) mount SMD components



2) prepare the 1:1 input and output baluns



3) mount the PCB on the copper heat spreader.



*Note: I have tested this design also with the MRF6VP2600H, and it works perfectly. However, this device is more fragile than the 5600H
In this version I used 4 x 5.1 pF with a small space in between.*

8) Before soldering the transistor it is preferred to perform some small tests.

- a) Set the bias potentiometer to zero.
- b) With a DVM (Digital Volt Meter) measure in the resistance between the gate pad and ground

$R = 30 \Omega$

9) Transistor placement :

Two techniques can be used:

- a) The transistor can be soldered. This technique is preferred to obtain a very low thermal resistance. Disadvantage is, when the transistor is destroyed for any reason it will be difficult to replace.
- b) Use silicon grease (the white one for a lower thermal resistance)

Before doing anything, the transistor has to be prepared.

As delivered, the flange of the transistor is not very "flat". To improve the flatness, the best way is to use abrasive paper type 3 M 734 "P1200".

The abrasive paper has to be put on a very flat surface, like glass.

Hold the transistor and make a shape of the number "8" with your hand until the flange is very flat.



Mount the transistor.

10) Bias adjustment

Connect the output to a 50 Ω load.

Use two power supplies:

One for the bias 0 to 12 V

Set to 5 V (check if the bias potentiometer is set to ground!!)

Set the drain power supply to 50 V and limit the current consumption to 2A.

Adjust the drain current (I_{dq}) up to 2A, i.e. each part of the LDMOS device draws 1A.

11) Small signal test:

If you have a network analyzer or similar, test the amplifier in small signal mode, otherwise with very low input power. Connect the output of the amplifier to an appropriate dummy load.

Tune the input VSWR by trimming L1 and C6.

The input return loss should be better than 15 dB.

The small signal gain is around 28 dB.

If you do not get this values **DO NOT** drive the amplifier to full power, you may have a wrong output wiring. Double check the input and/or output circuits thoroughly.

12) High power test:

A priori, these LDMOS devices are very sensitive towards overdrive. The best way to keep your transistor alive, is to attenuate the input power in all cases.

Nowadays 432 MHz transceivers have output powers around 50 W. Of course the output power can be lowered to 1 W. But... "if you forget", you will drive 50 W into the amplifier and destroy the transistors immediately.

Note: Many amateur transceivers with power controls have a bad ALC and may transmit a big spike at the beginning of each transmission.

Again, reduce the output power of your transceiver e.g. with a 10 dB (power) attenuator or a long length of e.g. RG316 coaxial cable.

Next step:

Inject ca. 1 W into the amplifier, and ca. 200 W output power should be measured. Check the drain current: it has to be approximately 10 A.

If it is not the case, **stop and verify the output matching circuit (i.e. balun and the capacitors).**

If all works well, increase the input power until 500 W of output power is achieved ($P_{in} = \sim 3.5W$) and optimize the efficiency with C23.

Also monitor and minimize the input VSWR.

Repeat this for each 500 W pallet.

Connect the two tested (and working!) pallets to both the input and output combiners. Inject sufficient drive (ca. 1.5W) to obtain ca. 200W output. Monitor the drain current: it should be around 14A.

If it is not the case, **stop and verify the combiner phases of both the input and output.**

If all works well, increase the input power to achieve 500 W output, and monitor the drain current: it has to be in the range of 23 A. The input power should be around 3.5W

Increase the input power until 1 kW output is reached (input ca. 10W). The total drain current should be around 32A.

Don't forget to use protection circuits. Several descriptions are available (3) (4)

A kit of the main components of this amplifier is available (5).

Conclusion

This design was duplicated several times before publication of this article, and each amplifier showed similar results.

However, be careful. High power amplifiers can be dangerous.

Many thanks to F1JRD Lionel, F1TE Lucien, F6BKI Jacques, Remco PA3FYM, Thomas Jann , F5VHX Graham

I want to mention a special memory of Rainer DJ9BV who in the mid 90's exchanged with me a lot of mail and discussion to create 1 kW 70 cm solid state.

And also some special thanks to Dick K2RIW, he showed me his first (1970's) "K2RIW" amplifier a kW on 70 cm when I visited him t10 years ago.

References

MRFE6VP5600H datasheet

(1) A compact 144 MHz High Power Solid State Amplifier using the MRFE6VP6125KH by F1JRD

(2) AN1034D Freescale (ex TRW application note)

(3) WWW.f1te.org ; WWW.f5cys.eklablog.com/

(4) WWW.vk4dd.com/

(5) WWW.rfham.com

(6) A compact 50 MHz High Power Solid State Amplifier using the MRFE6VP6125KH by F5FLN